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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/557,088 | 04/21/2000 | Hiroshi Sonabe | HYAE:097 | 6278 |

7590 04/02/2004

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| EXAMINER | |
|---|---|
| DOOLEY, MATTHEW C | |
| **ART UNIT** | **PAPER NUMBER** |
| 2133 | 15 |

DATE MAILED: 04/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/557,088 | SONABE, HIROSHI | |
| | Examiner | Art Unit | |
| | Matthew C. Dooley | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/17/04 has been entered.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endoh et al., U.S. 5,485,094, in view of Ferguson et al., U.S. 6,202,181 and Parker et al., U.S. 5,513,188.

As per claim 1:

Endoh teaches to a semiconductor inspection method that includes obtaining input logical values from the logical circuit such that the extracted data representing the adjacent lines have complimentary logical values (Fig.1: 10, 11: P3), as well as monitoring the output of a logical circuit that receives the input values and comparing the monitored output values with a set of expected data values (Fig.3: 35) for determination of short circuit occurrences between device lines (Col.1: 62-67). However, not explicitly taught by

Endoh is that the data representing specific lines of a logical circuit of a semiconductor apparatus represented by layout data should be extracted from the tested devices for avoiding a short circuit, wherein the aforementioned lines are adjacent to one another. Ferguson teaches to a method of short circuit and stuck at fault determination in semiconductor circuit testing wherein data is extracted representing adjacent lines of a logical circuit of a semiconductor apparatus represented by layout data for testing purposes (Col.10: 17-24; 45-47). It would have been obvious for one of ordinary skill in the art at the time of the invention to make use of the method of adjacent line testing taught by Ferguson with the testing method of Endoh because the method of Ferguson allows for fewer lines to have to be tested, thus leading to faster device testing (Col.10: 23-24). Endoh clearly and particularly demonstrates motivation for rapid testing and minimum pattern selection in the testing methodology (Col.1: 62-67), and thus, one skilled in the art would be motivated to combine the testing methodologies of the aforementioned references for faster circuit testing. Furthermore, as shown above, both Endoh and Ferguson teach to inputting values to a circuit for testing so that an expected logical output value is output by the logical circuit when no short circuit exists between adjacent tested lines, and an unexpected output logical value is output when a short circuit exists between adjacent lines, however neither Endoh nor Ferguson expressly teach to setting adjacent input lines of the logical circuit to logical values of 1 and 0, while setting the input values other than the two aforementioned lines to a logical value of 1 or 0. Parker teaches to setting adjacent input lines of the logical circuit to logical values of 1 and 0, while setting the input values other than the two aforementioned lines

to a logical value of 1 or 0 (Fig.4; Col.4: 44-57). It would have been obvious for one of ordinary skill in the art at the time of the invention to make use of the circuit testing test pattern disclosed by Parker for short circuit determination, because the implementation of the testing pattern disclosed by Parker allows for very good diagnostic resolution (Parker: Col.4: 57-58).

As per claim 2:

Claim 2 is similar in scope to that of claim 1, with the additional limitation of the extraction of data lines must be made when the distance between the lines is equal to or less than a threshold. Ferguson teaches to this additional limitation (Col. 10: 21-24). The remaining limitations are rejected using analogous reasoning to that used in the rejection of claim 1 above.

As per claim 3:

Claim 3 is analogous to claim 1 and as such, is rejected using analogous reasoning to that used in the rejection of claim 1 above.

As per claim 4:

Claim 4 is analogous in scope to claim 2 and as such, is rejected using analogous reasoning to that used in the rejection of claim 1 above.

***Conclusion***

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Dooley whose telephone number is (703) 306-5538. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matt Dooley

Matthew C. Dooley
Examiner AU 2133
03/31/04

Guy J. Lamarre for

Albert DeCady
Primary Examiner